



United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO. FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO. 5374	
09/927,129 08/10/2001		Enrique Musoll	P3828		
75	90 11/28/2005	EXAMINER			
JAMES W. H	UFFMAN	BANANKHAH, MAJID A			
HUFFMAN LA	W GROUP, P.C.				
1832 N. CASCADE AVE.			ART UNIT	PAPER NUMBER	
COLORADO S	PRINGS CO 80907	2105			

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		A	plication No.		Applicant(s)			
Office Action Summary		0	9/927,129		MUSOLL ET AL.			
		E	aminer		Art Unit			
			ajid A. Banankhah		2195			
Period fo	The MAILING DATE of this communica or Reply	ation appear	s on the cover sheet w	with the co	orrespondence ad	ldress		
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).								
Status								
1)⊠	Responsive to communication(s) filed	on 10 Augu	st 2001					
,								
,	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is							
<u>ا</u> رن	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Disnositi	on of Claims	u		,				
-		dia atia a						
	 4) Claim(s) 1-35 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 							
		withdrawn i	iom consideration.					
·	Claim(s) is/are allowed.							
·	Claim(s) <u>1-35</u> is/are rejected.				·			
·	Claim(s) is/are objected to.							
8)[_]	Claim(s) are subject to restriction	n and/or ele	ection requirement.					
Applicati	on Papers							
9)[The specification is objected to by the E	Examiner.						
10)	The drawing(s) filed on is/are: a)□ accepte	ed or b) objected to	by the E	xaminer.			
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).								
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority u	nder 35 U.S.C. § 119							
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 								
2) Notice 3) Notice	(s) e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO nation Disclosure Statement(s) (PTO-1449 or PT No(s)/Mail Date <u>01, 04, 05</u> .			o(s)/Mail Dat Informal Pa		D-152)		

Art Unit: 2195

DETAILED ACTION

This office action is in response to application filed on August 10, 2001. Claims 1-35 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C.

112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear what is meant by "characterized in that determination by the logic system that all ...and at least one of the context is idle". Is this "determination by the logic system" is part of any of the "determination logic" recited in the "first", and "second" logics, and if so, it is unclear which one it is referring to. In claim 14, in step (b), the claim recites: "[I]dle context within the singularly controlled group of contexts". The statement "the singularly controlled group of context" does not have proper antecedent basis. Appropriate correction is required.

In claim 13, "the priority rules" does not have proper antecedent basis. Additionally, it is unclear what is meant by "the priority rules used are based on <u>prediction of likely context assignment</u> of contexts released to the processing entity after release of the context for processing".

Art Unit: 2195

In claim 14, step (d), "the selected context" doe not have proper antecedent basis.

In claim 23, step (c), there is a gap between "not under control of the processor" in the preamble, and " now under processor control", which makes the step indefinite and incomprehensible.

Claims 2-13, 15-22, and 24-35 are rejected for the rejection of their base claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-11, 14, 16-33 are rejected under 35 U.S.C. 102(e) as being anticipated by **Muller** et al. (USP 6,483,804, hereinafter **Muller**).

As per independent claims 1, and 14:

Muller taught the invention as claimed including, a logic system in a data packet processor for selecting and releasing a context among a plurality of such contexts, claims 1, 14, and [claim 1/14, Fig. 1B, 142, Fig. 6A, 602 and 608, and Fig. 6B, 628], the selected and released context dedicated for enabling processing

Art Unit: 2195

of interrupt service routines corresponding to interrupts generated in data packet processing and pending for service [claim 1/14, Fig. 7, 712, and col. 50, lns. 17-24], the system comprising

a first determination logic for determining control status of all of the contexts [col. 29, lns. 54-68, "the status or condition of a packet"];

a second determination logic for determining if a context is idle or not [col. 67, lns. 6-29, "If the validity indicator is set, then there is a header buffer to receive this packet, and associated discussion"];

a selection logic for selecting a context [col. 67, lns., 6-29, "obtaining a free ring descriptor and retrieving its identifier (its reference to an available host memory buffer"]

a context release mechanism for releasing the selected context [col. 55., In. 66 to col. 56, In. 13, "In particular, it has been described above that when a memory buffer is released to a host computer it is identified to the host computer by its position within a free buffer array (or other suitable data structure) rather than by its buffer identifier. The host computer retrieves the buffer identifier from the specified array element and accesses the specified buffer to locate a packet stored in the buffer. As one skilled in the art will appreciate, identifying memory buffers in completion descriptors by the buffers' positions in a free buffer array can be more efficient than identifying them by their memory addresses. the descriptor is needed again"];

characterized in that determination by the logic system that all contexts are singularly owned by an entity not responsible for packet processing [claim 1/14, col. 57, ln. 53 to col. 58, ln. 8, "A distinction should be kept in mind between a buffer identifier (e.g., the memory address of a buffer) and the entry in the <u>free</u>

Art Unit: 2195

buffer array in which the buffer identifier is stored. In particular, it has been described above that when a memory buffer is released to a host computer it is identified to the host computer by its position within a free buffer array", and associated discussion],

and that at least one of the contexts is idle [claim 1/14, col. 67, lns. 6-29, "If the validity indicator is set, then there is a header buffer to receive this packet, and associated discussion"],

triggers immediate selection and release of one of the at least one idle contexts to an entity responsible for packet processing [claim 1/14(c and d), col. 55, ln. 66 to col. 56 ln. 13, "In particular, it has been described above that when a memory buffer is released to a host computer it is identified to the host computer by its position within a free buffer array (or other suitable data structure) rather than by its buffer identifier. The host computer retrieves the buffer identifier from the specified array element and accesses the specified buffer to locate a packet stored in the buffer. As one skilled in the art will appreciate, identifying memory buffers in completion descriptors by the buffers' positions in a free buffer array can be more efficient than identifying them by their memory addresses"].

As to independent claim 23:

A method for processing service routines associated in a data packet processing system [service routine, col., ln., and packet processing, col. 50, ln. 65 to col. 51, ln. 7] using a dedicated context selected among a plurality of contexts not under control of the processor comprising steps of [col. 50, ln. 65 to col. 51, ln., 7, "condition variable" may be used to indicate whether the thread has a packet to process."]:

(a) receiving at the processor, notification of a selected context

Art Unit: 2195

about to be released and memory marker pointing to an instruction thread in memory [col. 28, lns. 58-68, "Program 2300 begins with a WAIT instruction (e.g., instruction zero) that waits for a new packet (e.g., indicated by operator NP) and, when one is received, sets a parsing pointer to the twelfth byte of the layer two header."];

- (b) fetching the instruction thread designated by the received marker [col. 28, In. 58 to col. 29, In. 43, "a CLR_REG operation is conducted, but the operation enabler setting indicates that it is only conducted when the comparison succeeds (e.g., when a new packet is received"];
- (c) executing the instruction thread in the released context now under processor control [col. 29, lns. 44-53, "If the header is VLAN-tagged, the <u>pointer</u> is incremented a couple of bytes (e.g., one two-byte unit) and execution continues with <u>instruction</u> CFI; otherwise, execution continues with <u>instruction</u> 802.3", and associated discussion"];

As to dependent claim 2:

Muller taught the invention as claimed including when here is no idle context, all context being pre-loaded, aborting preloading of one context to render that context idle [**Muller**, col. 67, lns. 14-29, 1012 maintain a cache of descriptors referencing empty buffers, and associated discussions].

As to dependent claim 3:

Muller taught the invention as claimed including wherein the data packet processor is part of a data packet routing system [**Muller**, col. 9m, Ins. 42-54, load distributor 112 may determine which processor an incoming packet is to be <u>routed</u> to for processing through the appropriate protocol stack].

Art Unit: 2195

As to dependent claims 4, 16, and 25:

Muller taught the invention as claimed including wherein the data packet routing system is connected to a data packet network (**Muller**, Figs. 25A, and 25B].

Page 7

As to dependent claims 5, 17, and 26:

Muller taught the invention as claimed including wherein the data packet network is the internet network [Fig. 1A, and col. 11, lns. 1-13].

As to dependent claims 6, and 18-21:

Muller taught the invention as claimed including wherein the first and second determination logics and the selection logic and release mechanism are integrated on one hardware device [col. 34, In. 62 to col. 35, In. 4, "implemented in software or hardware device"].

As to dependent claims 7, and 18-21:

Muller taught the invention as claimed including wherein the hardware device is a register transfer unit [col. 25, Ins. 24-36].

As to dependent claim24:

Muller taught the invention as claimed including a step for calling and executing other service routines after all interrupts are serviced [col. 51, lns. 8-14, a cross-processor <u>call</u> is one way of communicating among processors whereby one processor is <u>interrupted</u> remotely by another processor.]

As to dependent claims 8, 22, 27, and 31-32:

Muller taught the invention as claimed including wherein a memory marker pointing to a memory address of a pre-defined instruction thread for invoking a stream to run in the released context [**Muller**, col. 29, lines 44-53].

Art Unit: 2195

As to dependent claims 9, and 33:

Muller taught the invention as claimed including wherein the selected and released context is dedicated to the serving of pending interrupts [col. 50, lns. 25-42].

As to dependent claims 10, and 28-29:

Muller taught the invention as claimed including wherein the memory containing the pre-defined thread is a cache memory used for containing program instructions [**Muller**, col. 56, lns. 20-30].

As to dependent claims 11, and 30:

Muller taught the invention as claimed including wherein the memory containing the pre-defined thread is a dedicated memory section of a processing core, the core also containing the contexts [col. 54, ln. 66 to col. 55, ln. 14, transfer of packet, from packet queue 116, into one or more buffer in host computer system].

Claim Rejections - 35 USC § 103

Claims12-13, 15, and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller in view of Tzeng (USP 6438135 hereinafter **Tzeng**).

As to dependent claims 12-13, and 34:

Muller discloses a method and system for selecting and releasing context that covers all limitations of parent claims. Muller discloses using multiple queues for multiple priority levels but does not explicitly show how packets are selected from queues based on priority.

Tzeng discloses a queuing switch and method for processing data packets transmitted through a network (Abstract).

Art Unit: 2195

Referring to Fig. 1-5, Tzeng shows an incoming packet processor 18 that creates an identifier EID for each incoming packet, assigns numbers to priority queues for storing the packets based on the created EID (clusters are numbered and priority for processing identified packets is by cluster number), and selects the packet from the queues based on the priority queue number (Col. 3, lines 48-50, and selection system selects packets for

processing based upon priority by queue number). Tzeng further discloses a weighted round robin technique for processing the various queues (Col. 5, lines 27-60, claim 14/33/52 - fairness algorithm is followed in selecting a queue within a priority cluster for selecting a packet for processing).

It would have obvious to one of ordinary skill in the art at the time of the invention to adapt the method and system of Muller by providing a number priority to cluster of queues for storing packets of multiple priority levels and selecting packets for processing based on the queue priorities using a fairness algorithm, as taught by Tzeng. This modification enables efficient storage and processing of data packets having different formats, protocols, and quality of service requirements.

As to dependent claims 15, and 35:

Muller taught the invention as claimed including a step (e) for processing low-priority tasks before releasing the selected context [col. 6, Ins. 49-68, "The switching fabric will then start to send data packets from the <u>low priority</u> queue 54 under the same operating procedure (arrow 62). Since the priority weight of the first data packet in the <u>low priority</u> queue 54 exceeds the service weight of that queue, the first service satisfied conditions is met for the <u>low priority</u> queue 54 and the switch fabric will return to servicing the high priority queue 48 (arrow 64)"]

Prior Art not relied upon

Art Unit: 2195

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

How to Contact the Examiner:

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Majid Banankhah, whose telephone number is 571-272-3770. A voice mail service is also available at this number. The Examiner can normally be reached on Monday-Friday, except Tuesdays from 7:00 AM - 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, An Meng-AI who can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

All responses sent by U.S. Mail should be mailed to:

Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

Art Unit: 2195

PTO CENTRAL FAX NUMBER: 703-872-9306

 Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

Majid Banankhah

11/17/05

MAJID BANANKHAH PRIMARY FRAMINER